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REMARKS

Claims 1 and 4-20 remain pending in the current Application. Claims 1, 4, 10, and 16 have been amended and claims 2-3 have been cancelled. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Drawing Objection under 37 C.F.R. 1.83(a)

Applicants submit that the drawings do show every feature of the invention specified in the claims. Again, the Examiner states that, with respect to claim 2, "the 'control circuitry' is claimed as an independent element from the 'instruction fetch unit'" and that "in FIG. 2, the 'control circuitry' is one of the elements inside the 'instruction fetch unit.'" (emphasis original). Therefore, the Examiner asserts that FIG. 2 does not show every feature of claim 2. However, Applicants respectfully disagree. Firstly, claim 2 claims the "control circuitry" (216) as an element within the central processing unit, regardless of whether it is located within the instruction fetch unit or not, and FIG. 2 clearly illustrates that control circuitry 216 is located within CPU 102, thus clearly showing this feature of claim 2. Furthermore, FIG. 2 illustrates just *one embodiment* where the control circuitry may be located in instruction fetch unit 220. That is, in alternate embodiments, the control circuitry may be located outside the instruction fetch unit, as clearly covered by claims 2-5 and 13 as filed, so long as it still provides the desired functionality. Therefore, Applicants submit that the drawings does show every feature of the invention specified in the claims..

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Rejection of claims 1, 2, 7-13, and 15-20 under 35 U.S.C. 102

Applicants respectfully submit that claims 1, 2, 7-13, and 15-20 are patentable over Great Britain Patent No. 2, 283, 595 (hereinafter referred to as GB '595)

Claims 1, 2, and 7-9

Applicants submit that claim 1 is not taught or suggested by GB '595. However, the Examiner has indicated that claim 3 would be allowable if rewritten in independent form; therefore, in order to further prosecution, Applicants have amended claim 1 to include the limitations of claim 3 and intervening claim 2. Applicants have cancelled claims 2 and 3, and have amended claim 4 to depend from claim 1 rather than cancelled claim 3. Therefore, as indicated by the Examiner, Applicants submit that claim 1 is patentable over GB '595.

Claims 7-9 have not been independently addressed because they depend directly or indirectly from allowable claim 1, and are therefore allowable for at least those reasons stated above with respect to claim 1.

Claims 10-13 and 15-20

Applicants submit that claims 10 and 16 are not taught or suggested by GB '595. Applicants have amended claims 10 and 16 to further clarify the address setup timing and not for prior art reasons. For example, with respect to claim 10, Applicants have clarified that the first mode of operation allows for a first address valid time corresponding to a first driven address, the first address valid time providing a first memory access time within a clock cycle in which the first address is driven. Applicants have also clarified that the second mode of operation allows for a second address valid time corresponding to a second driven address, the second address valid time providing for additional memory access time, as compared with the first memory access time, within a clock cycle in which the second address is driven. Applicants submit that this is not taught or suggested by GB '595. Note that claim 16 has been amended to also clarify the first and second modes with language similar to that used in claim 10; therefore, Applicants submit that the same arguments apply for both claims 10 and 16.

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For example, referring to FIGs. 4 and 5 (corresponding, for example, to the second mode of operation) results in an address valid time, $T_{AV, NOPRED}$ that is earlier in the clock cycle in which the branch target is driven as compared to FIGs. 6 and 7 (corresponding, for example, to the first mode of operation) which results in a later address valid time, $T_{AV, PRED}$ in the clock cycle in which the branch target is driven. Therefore, $T_{AV, PRED}$ provides for a greater memory access time for the branch target as compared to the memory access time provided by $T_{AV, NOPRED}$ since $T_{AV, PRED}$ occurs earlier in the clock cycle.

With respect to GB '595, the Examiner cites the single taken/not taken bit as the first signal which enables the first or second mode of operation. However, the states of the single taken/not-taken bit are used to predict whether the branch is taken or not and does not affect timing of the address valid time. That is, the single taken/not-taken bit is used to determine how to generate the next predicted address (whether it is a sequential address or a branch target address) where the timing of the next predicted address is not affected by this single taken/not-taken bit. The Examiner proceeds to cite "the first mode of operation utilizes branch prediction at the earlier time, see page 5, line 15". However, the "earlier time" cited on page 5, line 15, of GB '595 does not refer to two operating modes where one results in an earlier address valid time within the clock cycle of the driven address, but instead refers to the earlier time at which an address is predicted when using branch prediction (regardless of the branch prediction mode used). Furthermore, since branch prediction is used in both branch prediction modes in GB '595, both branch prediction modes result in a *same* address valid time. That is, there is no teaching or suggestion in GB '595 of two modes providing different memory access times within the a clock cycle in which the target addresses are driven. Therefore, GB '595 does not teach or suggest the elements of claims 10 and 16. Therefore, for at least these reasons, Applicants submit that claims 10 and 16 are patentable over GB '595.

Claims 11-13 and 17-20 all depend directly or indirectly from allowable claims 10 and 16 and are therefore allowable for at least those reasons described above with respect to claims 10 and 16.

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Rejection of claims 6 and 14 under 35 U.S.C. 103(a)

Applicants respectfully submit that claims 6 and 14 are patentable over GB '595 under 35 U.S.C. 103(a). Claims 6 and 14 depend directly or indirectly from allowable claims 1 and 10, respectively, and are therefore allowable for at least those reasons stated above with respect to claims 1 and 10, respectively. Furthermore, in rejecting claims 6 and 14 over GB '595 under 35 U.S.C. 103(a), the Examiner states that "using a signal being hardwired to a predetermined state to speed up signal process is old and well known in the art." The Examiner, in the Response to Arguments section of the current Office Action also states that "the motivation to speed up a signal process... is always there." However, Applicants submit that it would not be obvious to modify the signals of GB '595 to be hardwired to a predetermined state. While a hardwired signal may increase speed of a particular signal, it also *removes the flexibility of being able to change states of the signal*. The signals in GB '595 cited by the Examiner to perform branch prediction need to be able to toggle states in order to properly control the logic within data processor 10 of GB '595. Therefore, for these additional reasons, claims 6 and 14 are patentable over GB '595.

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Conclusion

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

Please charge any fees due to Deposit Account Number 502117, Motorola, Inc..

Respectfully submitted,

SEND CORRESPONDENCE TO:

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